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EXAMINER	
KE, PENG	

ART UNIT	PAPER NUMBER
2174	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application	Applicant(s)	
	09/742,523	ROGERS ET AL.	
	Examiner	Art Unit	
	Peng Ke	2174	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communications: Amendment, filed on 12/18/03.

2. Claims 1-43 are pending in this application. Claims 1, 8, 15, 23, 30, and 37 are independent claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5-11, 13-16, 36, 37, 39-43, 45-47 are rejected under 35 U.S.C. 102(b) as being anticipated by McKaskle et al. (US 5,481,741).

As per claim 1, McKaskle et al. teaches a method for creating a graphical program which performs register accesses in a hardware device, wherein the method operates in a computer including a display screen and a user input device (col. 5, lines 46-61), the method comprising:

displaying on the screen a register access node in the graphical program in response to user input (fig. 99, col.49, lines 49-56); and

configuring the register access node to access one or more registers of a hardware device (fig. 99, col.49, lines 49-56);

wherein, during execution of the graphical program, the register access node is operable to access the one or more registers of the hardware device. (fig 13, col 26, lines 2-27)

As per claim 3, McKaskle teaches the method of claim 1, further comprising:

storing a description of the hardware device in the computer;

wherein the register access node uses the description of the hardware device to access registers of the hardware device during execution of the graphical program (col. 31, lines 34-67) It is inherent that the description of the hardware will be stored within the computer in order to correctly simulate the execution state.

As per claim 5, McKaskle teaches the method of claim 3, wherein the description includes mnemonic names of registers; wherein said configuring the register access node includes:

displaying a list of the mnemonic names of registers on the display; and receiving user input selecting one or more of the mnemonic names of registers for access (Fig 90, item DBL).

As per claim 6, McKaskle teaches the method of claim 5, wherein the description further includes mnemonic names of fields in the registers;

wherein said configuring the register access node includes:

displaying a list of the mnemonic names of fields in the registers on the display; and

receiving user input selecting one or more of the mnemonic names of fields in the registers for access (Fig. 89, items "vi", "Trig &log", and "file i/o"...).

As per claim 7, McKaskle et al. teaches the method of claim 1, wherein said configuring the register access node comprises:

displaying an icon on the graphical program which references register access node configuration information (fig. 19g, items DBL and Wave); and

connecting the icon to the register access node.

As per claim 8, McKaskle et al. teaches the method of claim 7, wherein the icon is a hardware open node (fig. 19g, items DBL and Wave).

As per claim 9, McKaskle et al. teaches the method of claim 1, wherein said register access node comprises one or more input terminals, the method further comprising:

configuring the one or more input terminals to write a register of the hardware device (fig. 80, col. 64, line 15-21, col. 46, lines 16-34).

As per claim 10, McKaskle et al. teaches the method of claim 1, wherein said register access node comprises one or more output terminals, the method further comprising:

configuring the one or more output terminals to read a register of the hardware device (fig. 111, 112, col. 51, lines 25-49)

As per claim 11, McKaskle et al. teaches the method of claim 1, further comprising:

displaying on the screen a first node in response to user input, wherein the first node references the hardware device (fig. 80, col. 64, line 15-21, col. 46, lines 16-34); and

connecting the first node to the register access node, wherein said connecting provides the register access node with information regarding the hardware device (col. 46, lines 60-68, col. 47, lines 1-14).

As per claim 13, McKaskle et al. teaches the method of claim 11, wherein said connecting the first node to the register access node includes displaying on the screen a wire connecting the first node to the register access node (fig. 75, item wire).

As per claim 14, McKaskle et al. teaches the method of claim 1, further comprising:

constructing execution instructions in response to the graphical program, wherein the execution instructions are executable to access registers of the hardware device (col. 31, lines 34-55).

As per claim 15, McKaskle et al. teaches the method of claim 14, further comprising:

executing said execution instructions, wherein the register access node accesses registers of the hardware device during said executing (col. 31, lines 34-55).

As per claim 16, McKaskle et al. teaches the method of claim 1, wherein the graphical program is operable to access registers of the hardware device for performing instrumentation functions on an instrument (col 33, lines 49-61).

As per claim 36, McKaskle et al. teaches a method for creating a graphical program which performs register accesses in a hardware device, wherein the method operates in a computer including a display and a user input device, the method comprising:

storing a description of a hardware device (col. 14, lines 63-68);

displaying on the screen a register access node in the graphical program in response to user input, wherein the register access node is operable to access the hardware device (fig. 99, col.49, lines 49-56);

connecting an input of the register access node to receive a description of a hardware device in response to user input (fig. 99, col.49, lines 49-56); and

configuring the register access node to access selected registers described in the description of the hardware device in response to user input (fig. 99, col.49, lines 49-56);

wherein the register access node is operable to access the selected registers of the hardware device during execution of the graphical program (fig 13, col 26, lines 2-27).

As per claim 37, McKaskle et al. teaches a memory medium for performing register accesses in a hardware device, the memory medium comprising program instructions executable to:

display on the screen a register access node in the graphical program in response to user input (fig. 99, col.49, lines 49-56); and

configure the register access node to access one or more registers of a hardware device (fig. 99, col.49, lines 49-56);

wherein, during execution of the graphical program, the register access node is operable to access the one or more registers of the hardware device (fig 13, col 26, lines 2-27).

As per claim 39, McKaskle et al. teaches the memory medium of claim 37, further comprising program instructions executable to:

store a description of the hardware device in the computer (col. 14, lines 63-68);

wherein the register access node uses the description of the hardware device to access registers of the hardware device during execution of the graphical program (col. 14, lines 63-68). It is inherent during the execution the process will follow the description of the hardware device.

As per claim 40, McKaskle et al. teaches the memory medium of claim 39, wherein said configuring the register access node to access one or more registers of the hardware device comprises configuring the register access node to access selected registers described in the description of the hardware device (fig. 99, col.49, lines 49-56).

As per claim 41, it is of the same scope as claim 7. (see rejection above)

As per claim 42, it is of the same scope as claim 14. (see rejection above)

As per claim 43, McKaskle et al. teaches a system for performing register accesses in a hardware device, the system comprising:

a computer including a processor coupled to a memory (col. 13, lines 56-68);

a hardware device coupled to the computer (col. 13, lines 56-68);

wherein the processor is operable to execute program instructions stored in the memory to:

display on the screen a register access node in a graphical program in response to user input (fig. 99, col.49, lines 49-56); and

configure the register access node to access one or more registers of the hardware device (fig. 99, col.49, lines 49-56);

wherein, during execution of the graphical program, the register access node is operable to access the one or more registers of the hardware device (fig 13, col 26, lines 2-27).

As per claim 45, which is dependent on claim 43, it is of the same scope as claim 39. (see rejection above)

As per claim 46, which is dependent on claim 45, it is of the same scope as claim 40. (see rejection above)

As per claim 47, it is of the same scope as claim 7. (see rejection above)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 38, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over McKaskle (US 5,481,741) in view of Sojoodi et al. (US 5,847,953).

As per claim 2, McKaskle et al. teaches the method of claim 1.

However McKaskle et al. fails teaches wherein said configuring the register access no de includes: displaying a list of registers; and

receiving user input to select one or more of the registers from the list of registers.

Sojoodi et al. teaches a system that configures the register access node includes: displaying a list of registers (Fig 7, col. 17, lines 17-46); and

receiving user input to select one or more of the registers from the list of registers (Fig 7, col. 17, lines 17-46).

It would have been obvious to an artisan at the time of the invention to include Sojoodi et al.'s teaching with McKaskle et al.'s system in order to allow the user to easily configure and select a specific register.

As per claim 38, McKaskle et al., teach the memory medium of claim 37. However they fail to teach a memory medium wherein in performing said configuring the register access node, the program instructions are executable to:

display a list of registers; and

receive user input to select one or more of the registers from the list of registers.

Sojoodi et al. teaches a system a memory medium wherein in performing said configuring the register access node, the program instructions are executable to:

display a list of registers; and

receive user input to select one or more of the registers from the list of registers.

(Fig 7, col. 17, lines 17-46).

It would have been obvious to an artisan at the time of the invention to include Sojoodi et al.'s teaching with system of McKaskle in order to allow user to easily configure and select a specific register.

As per claim 44, which is dependent on claim 43, it is of the same scope as claim 38. (see rejection above)

Claims 4, 12, 17, 18, 23-25, 29, and 30-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over McKaskle (US 5,481,741) in view of Yamamoto et al. (US 5,847,953).

As per claim 4, McKaskle teaches the method of claim 3. However McKaskle et al. fails to teach the method wherein said configuring the register access node to access one or more registers of the hardware device comprises configuring the register access node to access selected registers described in the description of the hardware device.

Yamamoto et al. teach a method wherein said configuring the register access node to access one or more registers of the hardware device comprises configuring the register access node to access selected registers described in the description of the hardware device (col. 10, lines 12-25).

It is inherent that in order to transfer the protocol to the input device, the server must configure the register hardware device. It would have been obvious to an artisan at the time of

the invention to include Yamamoto et al.'s teaching with McKaskl et al.'s system in order to allow the user to operate the registered hardware device using GUI.

As per claim 12, McKaskle teaches the method of claim 11. However he fails to teach the method wherein the first node is a hardware refnum node which references a description of the hardware device (It is implicit for McKaskle to further define each hardware node, because there are a plurality of same hardware nodes present in his invention (Fig. 80)). Yamamoto et al. teaches a method wherein the first node is a hardware refnum node which references a description of the hardware device. (Fig. 9A, items 47, 1, 2, 3, col. 10, liens 37-68) It would have been obvious to an artisan at the time of the invention to include Yamamoto et al.'s teaching with system of McKaskle in order allow the user to further define the hardware device when there is a plurality of the same device present in the system.

As per claim 17, McKaskle et al. teaches a method for creating a graphical program which performs register accesses in a hardware device, wherein the method operates in a computer including a display and a user input device, the method comprising:

storing a description of a hardware device (col. 56, lines 10-18);

displaying on the screen a first node in response to user input, wherein the first node references the description of the hardware device (col. 56, lines 19-24);

displaying on the screen a register access node in response to user input, wherein the register access node is operable to access the hardware device (col. 62, lines 16-40) ;

connecting the first node to the register access node in response to user input, wherein the first node is operable to provide the description of the hardware device to the register access node (col. 56, lines 19-24);

However, McKaskle et al. fails to teaches the program

wherein the register access node receives the description, wherein the register access node is operable to access registers of the hardware device during execution of the graphical program.

Yamamoto et al. teaches a system wherein the register access node receives the description, wherein the register access node is operable to access registers of the hardware device during execution of the graphical program (col. 10, lines 12-25).

It would have been obvious to an artisan at the time of the invention to include Yamamoto et al.'s teaching with McKaskl et al.'s system in order to allow the user to operate the registered hardware device using GUI.

As per claim 18, McKaskle et al. and Yamamoto et al. teach the method of claim 17. Yamamoto further teaches the method comprising:

configuring the register access node to access selected registers described in the description of the hardware device (fig. 27A, items "my digital camera", "engineer fax"...).

It would have been obvious to an artisan at the time of the invention to include Yamamoto et al.'s teaching with McKaskl et al.'s system in order to allow the user to identify the node with the hardware.

As per claim 23, which is dependent on claim 17, it is of the same scope as claim 18. (see rejection above)

As per claim 24, McKaskle et al. and Yamamoto et al. teach the method of claim 17. Yamamoto et al. further teaches wherein said register access node comprises one or more input terminals, wherein, for each input terminal, the method further comprises:

configuring each input terminal to write a register of the hardware device (fig. 27A, items "my digital camera", "engineer fax"...). It is inherent when the instructions are written to the hardware devices, the register of the hard ware device are accessed and written over.

It would have been obvious to an artisan at the time of the invention to include Yamamoto et al.'s teaching with McKaskl et al.'s system in order to allow the user to identify the node with the hardware.

As per claim 25, McKaskle et al. and Yamamoto et al. teach the method of claim 17, Yamamoto further teaches wherein said register access node comprises one or more output terminals, wherein, for each output terminal, the method further comprises:

configuring said each output terminal to read a register of the hardware device (col. 12, lines 35-49).

As per claim 29, McKaskle et al. and Yamamoto et al. teaches the method of claim 17, , McKaskle et al. further teaches wherein the first node is a hardware open node (fig. 100 B, item "7").

As per claim 30, which is dependent on claim 29, it is of the same scope as claim 12. (see rejection above)

As per claim 31, which is dependent on claim 17, it is of the same scope as claim 12. (see rejection above)

As per claim 32, McKaskle et al. and Yamamoto et al. teach the method claim 17, McKaskle further teaches wherein said connecting the first node to the register access node includes displaying on the screen a wire connecting the first node to the register access node (Fig. 9A, item "A").

As per claim 33, which is dependent on claim 17, it is of the same scope as claim 24. (see rejection above)

As per claim 34, which is dependent on claim 33, it further teaches the method of claim 33, further comprising:

executing said execution instructions, wherein the register access node accesses registers of the hardware device during said executing (col. 10, lines 26-37).

As per claim 35, McKaskle et al. and Yamamoto et al. teach the method claim 17. McKaskle further teaches wherein the graphical program is operable to access registers of the hardware device for performing instrumentation functions on an instrument (col. 10, lines 26-37).

Claims 19-22, and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over McKaskle (US 5,481,741) in view of Yamamoto et al. (US 5,847,953) further in view of McIntyre et al. (US 6,229,538).

As per claim 19, McKaskle et al. and Yamamoto et al. teach the method of claim 18. However they fail to teach the method wherein said configuring the register access node includes:

displaying a list of registers described in the description of the hardware device;

receiving user input to select one or more of the registers from the list of registers.

McIntyre et al. teaches a system wherein said configuring the register access node includes:

displaying a list of registers described in the description of the hardware device;

receiving user input to select one or more of the registers from the list of registers (Fig 5, col. 8, lines 38-64).

It would have been obvious to an artisan at the time of the invention to include McIntyre et al.'s teaching with system of McKaskle and Yamamoto in order to allow user to easily configure and select a specific register.

As per claim 20, McKaskle et al., Yamamoto et al. and McIntyre et al teach the method of claim 19. McIntyre further teaches the method wherein the description includes mnemonic names of registers;

wherein said configuring the register access node includes:

displaying a list of the mnemonic names of registers on the display (fig. 5, items d1-d4); and

receiving user input selecting one or more of the mnemonic names of registers for access (col. 8, lines 36-64).

As per claim 21, McKaskle et al., Yamamoto et al. and McIntyre et al teach the method of claim 20, McKaskle further teaches further comprising:

displaying selected mnemonic names of registers on the display after said receiving user input selecting one or more of the mnemonic names of registers for access (fig. 100 B, item "7")

It is inherent the value represent by "7" which is the last value passed will continue to be updated after receiving user's input.

As per claim 22, McKaskle et al., Yamamoto et al. and McIntyre et al teach the method of claim 20, wherein the description further includes mnemonic names of fields in the registers;

McIntyre further teaches wherein said configuring the register access node includes:

displaying a list of the mnemonic names of fields in the registers on the display; and

receiving user input selecting one or more of the mnemonic names of fields in the registers for access (Fig 5, items d1-4, col. 8, lines 37-64).

As per claim 26, McKaskle et al. and Yamamoto et al. teach the method of claim 17. However they fail to teach the method wherein receiving user input further comprises:

selecting a first register from said list of registers;

associating a first terminal of the register access node with said first register;

selecting the first terminal as a read or a write terminal;

connecting the first terminal to a node in the graphical program; and

repeating the above steps for one or more registers of the hardware device.

McIntyre et al. teaches a system wherein receiving user input further comprises:

selecting a first register from said list of registers;

associating a first terminal of the register access node with said first register;

selecting the first terminal as a read or a write terminal;

connecting the first terminal to a node in the graphical program; and

repeating the above steps for one or more registers of the hardware device (Fig 5, items d1-4, col. 8, lines 37-64).

It would have been obvious to an artisan at the time of the invention to include McIntyre et al.'s teaching with system of McKaskle and Yamamoto in order to allow user to easily configure and select a specific register.

As per claim 27, McKaskle et al., Yamamoto et al. and McIntyre et al teach the method of claim 26, McKaskle et al. further teaches wherein the register access node is a grow able node which may comprise a variable number of user selected terminals (fig. 100 B, item "7").

As per claim 28, which is dependent on claim 17, it is of the same scope as claim 26. (see rejection above)

Response to Argument

Applicant's argument filed on claim 1 has been fully considered but they are not persuasive.

Applicant's primary argument includes the following:

A) McKaskle fails to teach hardware device registers.

B) Microsoft dictionary defines hardware register to be a set of memory within a microprocessor or other electronic device used to hold data for a particular purpose. Therefore, the shift register taught by Mckaskle (col. 49, lines 49-56) fits the definition of a hardware register, since it holds data within an electronic device.

Applicant's arguments with respect to claims 18-22, and 26-28 have been considered but are deemed to be moot in view of the new grounds of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peng Ke whose telephone number is (703) 305-7615. The examiner can normally be reached on M-Th and Alternate Fridays 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kristine L Kincaid can be reached on (703) 308-0640. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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